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(54) Accelerator architecture for a speech codec

(57) A codec (110) comprising a programmed digital signal processor (112) and an accelerator core (116) in which computation of a coding algorithm is divided between the digital signal processor (112) and the accel-

erator core (116), computationally relatively intensive parts of a coding algorithm being performed by the accelerator core. In the preferred embodiment, the instruction set is optimised to perform CELP coding of speech signals.

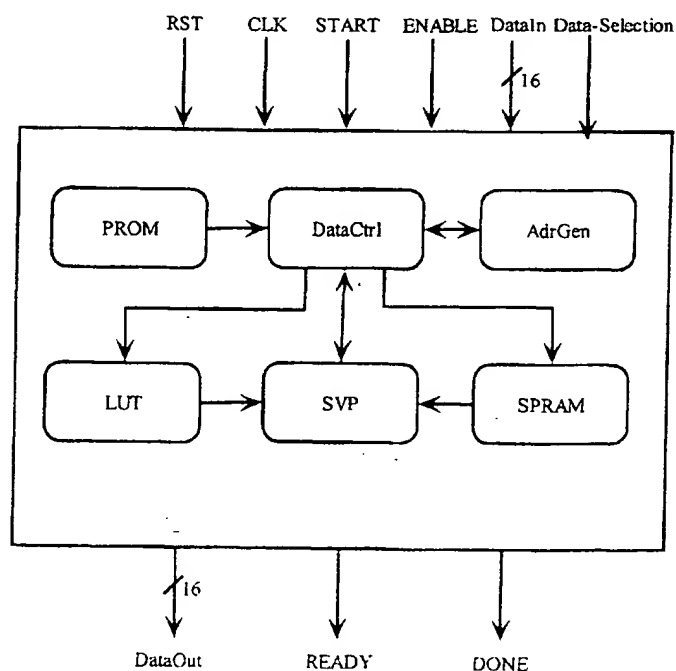


Fig 2

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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO.

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Application Number

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
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Place of search	Date of completion of the search	Examiner	
MUNICH	3 February 2004	Zimmermann, E	
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<p>X : particularly relevant if taken alone</p> <p>Y : particularly relevant if combined with another document of the same category</p> <p>A : technological background</p> <p>O : non-written disclosure</p> <p>P : intermediate document</p>			

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